WHAT IS CLAIMED IS:

1. A PWM signal generating circuit comprising:

a first counter circuit periodically changing a PWM signal output therefrom into an active state; and

a second counter circuit changing the PWM signal, which has been changed into the active state by said first counter circuit, into an inactive state within each cycle,

wherein said second counter circuit increases and decreases an active-to-inactive time period from a time when the PWM signal is changed into the active state to a time when the PWM signal is changed into the inactive state.

2. The PWM signal generating circuit as claimed in claim 1, wherein the PWM signal circuit consists of a plurality of circuit elements each of which outputs a digital signal.

3. The PWM signal generating circuit as claimed in claim 1, further comprising a first specifying circuit that specifies an upper limit value and a lower limit value, wherein said second counter circuit changes the active-to-inactive time period periodically within a range between the upper limit value and the lower limit value.

4. The PWM signal generating circuit as claimed in claim 3, further comprising a second specifying circuit that specifies a first schedule time and a second schedule time, wherein said second counter circuit starts to decrease the active-to-inactive time period after the active-to-inactive time period reaches the upper limit value and the first schedule time has elapsed, and said second counter circuit increases the active-to-inactive time period after the active-to-inactive time period reaches the lower limit value and the second schedule time has elapsed.

5. A method of generating a PWM signal, comprising the steps of:

periodically changing the PWM signal into an active state; and

changing the PWM signal, which has been changed into the active state, into an inactive state within each cycle, while changing an active-to-inactive time period from a time when the PWM signal is changed into the active state to a time when the PWM signal is changed into the inactive state.

6. The method as claimed in claim 5, wherein said step of changing includes changing the active-to-inactive time period periodically within a range between an upper limit value and a lower limit value.

7. The method as claimed in claim 6, wherein said step of changing includes decreasing the active-to-inactive time period after the active-to-inactive time

period reaches the upper limit value and the first schedule time has elapsed, and increasing the active-to-inactive time period after the active-to-inactive time period reaches the lower limit value and the second schedule time has elapsed.

8. A PWM signal generating circuit comprising:

first counter means for periodically changing a PWM signal output therefrom into an active state; and

second counter means for changing the PWM signal, which has been changed into the active state by said first counter means, into an inactive state within each cycle,

wherein said second counter means increases and decreases an active-to-inactive time period from a time when the PWM signal is changed into the active state to a time when the PWM signal is changed into the inactive state.

9. The PWM signal generating circuit as claimed in claim 8, wherein the PWM signal generating circuit consists of a plurality of circuit elements each of which outputs a digital signal.

10. The PWM signal generating circuit as claimed in claim 8, further comprising first specifying means for specifying an upper limit value and a lower limit value, wherein said second counter means changes the active-to-inactive time period periodically within a range between the upper limit value and the lower limit value.

11. The PWM signal generating circuit as claimed in claim 10, further comprising second specifying means for specifying a first schedule time and a second schedule time, wherein said second counter means starts to decrease the active-to-inactive time period after the active-to-inactive time period reaches

the upper limit value and the first schedule time has elapsed, and said second counter means increases the active-to-inactive time period after the active-to-inactive time period reaches the lower limit value and the second schedule time has elapsed.